

ALARC Approach for Litho Friendly Standard Cell Layout Design

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Abstract — The Shrinking geometries and shortening time-to-market are characteristics of contemporary semiconductor technologies. As the device dimension is moving towards deep submicron technology node, the gap between drawn & actual printed device size increases because of Lithographic effects and process variation which results in yield as well as performance degradation. In this paper we are describing, ALARC (Adaptive Lithography aware Regular Cell Design) approach for standard cell layout design which will reduce lithographic effects and will improve yield.

Keywords – Adaptive Lithography, Deep Submicron Technologies, Layout Design, ALARC Approach.

I. INTRODUCTION

Over the years, CMOS technology has scaled down and has enabled the production of increasingly complex products at lower cost, as Moore's Law predicted [7]. In modern technologies device size is reaching to few nanometer (i.e. 10nm, 7nm etc) with extremely complex lithography process to meet the challenging customer specification in terms of area, speed, power, along with yield and signal integrity. According to the Moore's Law, the cost of the chip should reduce, as the number of components that can be integrated on a single chip has increased tremendously. However, deep sub-micron technologies has increased the design-process interdependencies and process variations that are influencing both integrated circuit (IC) performance and yield [1], this increased complexities has led to increase in the cost per chip.

In order to maintain circuit performance and high yield, these variations must be mitigated or at least taken into account during the circuit and layout design stage to fully realize its potential and make the modification in the design accordingly [10]. As the technology node shrinks, the yield of the design is affected more because of the lithography and various manufacturing process variation which occurs at various fabrication steps.

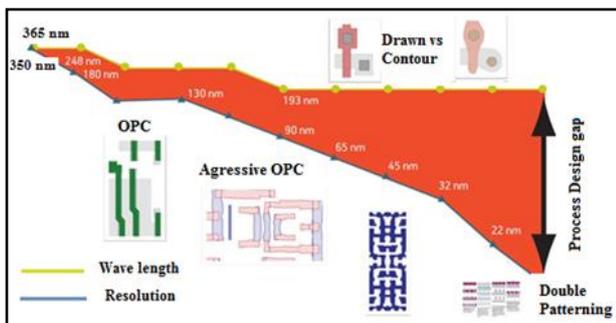


Fig.1. Process Design Gap (Figure shows drawn Vs printed gap increases as we move towards smaller device size)

The figure1 simply gives an idea that as the device dimension is narrowing down the relative variation between drawn versus printed is increasing constantly [11]. So to improve the printability, design must be modified at early stages for possible failures by taking into account the various lithographic effects and process related variations. If DFM measures are taken at early stages than it will save design time, efforts and cost as well. For this it is important to understand the various failure mechanisms that lead to performance and yield loss.

DFM is not a new thing for manufacturing process, many of these guidelines like double contact/via, spacing out metals, poly etc has been there since inception of VLSI industry [12]. However it has become now mandatory step of design process in nano meter technology node. The DFM rules are typically developed during process characterization or derived from experience learned from earlier technology nodes. To make the standard cell library DFM compliant at early stage of design is always a better approach, if the delay increases than simultaneously the design time and cost will also increase. A structured approach is needed in order to deal with the fundamental issue of variation in manufacturing process from what is designed, what are pattern which are going to be impacted [2]. In this work, brief background of DFM techniques, causes of yield loss and ALARC approach for improving the design to limit yield limiting design pattern is mentioned in detail. ALARC approach is merely guidelines; there can be cases where we will not be able to apply all the guidelines because of the complexity of the cell. But still, this method will be useful in most of the cases.

II. FAILURE MECHANISM

Semiconductor products are manufactured in high volume and their repair is impractical. The failure of one component may turn into a much bigger problem if the faulty component is used many times, as this leads to a

higher defect density [9]. Therefore, incorporation of reliability at the design stage and reduction of variation in the production stage have become essential. One step towards preventing failures is to analyze the likelihood of their occurrences. Since variability of failures is a major concern, it is generally statistically analyzed. Various models may be proposed based on detailed defect density analyses, which can then be customized for a particular design. The Failure mechanism can be divided in following categories:

A. Random Defects

Random defects are the dominant yield loss mechanism at larger technologies. Despite constant clean room improvements, particles still land on chips or masks. These particles cause catastrophic failures – shorts (extra metal between two metal lines) or opens (missing metal) – or result in parametric issues – resistive pinching, added coupling, etc [5]. In Figure 2(a) and 2(b), Random Defects, two of the most common random defects an Open Defect and a Short Defect are shown. Particles of different sizes randomly fall on the wafer to cause these Open Defects or Short Defects depending on the conductivity of the particle.

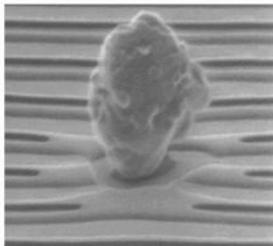


Fig.2. (a)

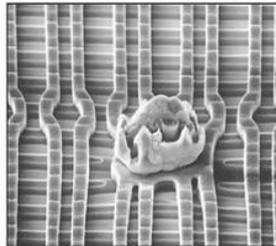


Fig.2. (b)

Random defects can be defined as any deviation from original design and only affect yield under specific circumstances. We can minimize the effects of random defect by keeping clean environment at fab; however we cannot neglect its impact completely.

B. Systematic Defects

Systematic yield issues are not random, but the result of interaction between the layout and process variations. These include chemical variations in materials; mechanical variations in CMP, optical variations in lithography, and plasma variations in etch [6]. Some examples of systematic defects are: planarity (the difference in metal heights for a given area on a design), antenna effects (charge accumulation of interconnect components), via opens, and electro migration.

C. Parametric Defects

The biggest issue for nanometre-scale designs is considered to be parametric yield loss [4]. This is when all elements of a chip are functioning, but timing or other electrical requirements, such as power, are not to specification. They are the result of interconnect parasitic and device physics, and can cause a circuit to behave in non-ideal ways, leading to effects such as power bus voltage drop, increased noise, and timing skew in clock and signal lines.

Out of these, parametric defects can be reduced by taking care of critical signals while designing, using Decap cell to remove supply noise, and STI to minimize leakage. While systematic and random defect will certainly cause some yield loss but these are minimized by making changes in layout based on Lithography simulation of the design.

III. LITHO FRIENDLY DESIGN

In deep submicron tech nodes design does not end only with physical verification (DRC/LVS). After DRC/LVS verification certain modification are done based on rule based approach (DRC + 10-25% of DRC) and then model based approach (Lithography simulation) is done to enhance the manufacturability of the design [11]. In the first approach, design is simulated for possible layout modifications and the simulation results are in terms of DFM score for each rule. We try to minimize DFM score corresponding to all rules as low as possible while keeping the area of the standard cell unchanged. DFM score for various design rules can be customized according to the type of application.

In the second approach, lithography simulation of the standard cell library is done which gives prediction of possible design failures for various process variations which might occur. LFD simulation is used to detect hotspots in the design [10]. Hotspots are those parts of the layout where possibility of failure because of lithographic effects and various process variations is more. LFD models are used for the simulations which are based on the inputs from the fab experts and test engineers. By LFD simulation we improve critical areas of the design which are prone to failure without violating DRC's and keeping the area unchanged.

However simulation results are highly influenced by the surrounding environment of the cell, denser the context made for LFD simulation, the better will be the results but at the same time simulation time increases since LFD flow includes making changes based on simulation results [3], than again running simulation for possible errors after the modifications than finally physical verification (DRC/LVS). So if we adopt approach like ALARC (Adaptive Litho Aware Regular cell Design) during design time along with LFD simulation it will be more robust way to minimize yield loss and will reduce design time.

IV. ALARC

Since LFD simulation results are highly influenced by the surrounding environment of the cell, denser the context the better will be the results but at the same time simulation time increases since LFD flow includes making changes based on simulation results, than again running simulation for possible errors after the modifications than finally physical verification (DRC/LVS). Number of iteration increases in conventional design process hence the design time. So if we adopt approach like ALARC

(Adaptive Litho Aware Regular cell Design) during design time itself along with LFD simulation than it will be more robust way to minimize yield loss and will reduce design time significantly [3]. However ALARC approach is merely guidelines, there can be cases where we will not be able to apply all the guidelines because of the complexity of the cell. But still, this method will be useful in most of the cases.

Advantages of ALARC approach:

1. LFD simulation is highly context dependent. Same cell will give different results in different environment, so making layouts while keeping ALARC guidelines in mind will be more robust way for litho friendly cell design.
2. As LFD simulation of libraries take hours of time, after modification in layouts for simulation errors, we again check for further LFD violation and than physical (DRC/LVS) verification, so if we adopt ALARC approach while designing we can reduce design time significantly. ALARC guidelines can be said as advanced guidelines for layout designing and is based on our experience of Lithography simulation of various libraries in 40 and 45 nm using Mentor graphics Calibre LFD kit. However these guidelines can be used in lower technology nodes also to make Litho friendly layouts. These guidelines are:

1. CMOS gate (poly) configuration

- Gates must be surrounded side by side by other poly lines to minimize the gate length narrowing. All diffusion strips must be surrounded side by side by dummy poly lines.
- Poly lines must be equally spaced so systematic poly-induced variations affect equally throughout all poly lines (regularity constraint). Hence, the across chip line-width variation (ACLV) between transistors is minimized.

2. Contacts and Via enclosures.

- Diffusion Contacts: Source/Drain contacts must be properly enclosed by the active region in order to avoid them to fall outside the oxide strip.
- Poly contacts: Poly contacts must be perfectly surrounded by the poly region extension created specifically for this connection to enhance the reliability of the input connection.
- Vias and contacts: Metal lines must be wide enough so that vias and contacts do not fall outside the metal layers and diffusion strips.
- Power rail vias: Wider metal lines (e.g. the power supply rails) require a wider enclosure to avoid vias falling outside the metal layer. In order to avoid this problem, we can connect vias on top of the substrate contacts, i.e., half pitch displaced from the routing grid so vias will be inside the power supply.

3. Input placement.

- The shape of the poly contact enclosure should be rectangular, aligned with the poly shape and avoiding an abrupt change in poly width which might cause the poly gate to pinch.
- The number of poly contacts must be minimized in order to decrease the number of poly irregularities.

- Poly contacts are preferably placed on the ends of the poly gate to avoid the double narrowing / widening effect.
- Inputs should be placed far enough from the active region in order to obtain a regular line pattern resolution in the channel region.

4. Poly extension:

The poly gate end without a poly contact should be sufficiently extended so the line-end rounding will fall outside the active region

5. Metal Connections.

- Metal shapes are unidirectional in order to avoid proximity effects such as corner rounding or pinching due to hammerhead shapes.
 - Spacing must be properly designed in order to avoid shorts between contiguous metal lines. Additionally, metal lines must be equally spaced in order to maximize regularity and routability second.
1. Active regions can contain any number of equal width transistors. However, Very Small width transistors should not be shared with large transistors to avoid Active rounding. Here the impact of active rounding changes the width of small transistor and hence circuit performance.
 2. Signal Integrity: To maintain the signal integrity we try to avoid long metal connection parallel to supply rail as crosstalk is introduced because of the surrounding environment of the cell.
 3. Avoid higher metals: In our design we try to avoid higher metals like M2 and onwards as use of higher metal increases process complexity.

V. CONCLUSION & FUTURE SCOPE

Integrated circuit design is moving into the nanoscale era towards more compact, higher performance and lower power devices. Because of the increased complexity, Lithography effects and various process related constraint, there will always be some yield loss and negative impact on the performance of the circuit. However by adopting ALARC like approach during Layout development phase along with available DFM tools will be more fruit full method to suppress yield limiting design patterns and to reduce design time.

In future technology nodes, the size of the device will shrink more and hence complexity, so the DFM becomes more important. Many of the ALARC guidelines like Poly at regular pitches, regular diffusion strips etc are followed strictly, however this approach i.e. 'Making design changes which will counterbalance the manufacturing process variation' will be less useful as we will reach to the extreme of nanometre range (i.e. 20 nm or below). In this case, yield can only be improved by Wavelength extension, Process innovation and use of novel materials along with incorporating ALARC like guidelines and learning from DFM/LFD simulation as strict design rules.

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AUTHOR'S PROFILE



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He was born in District Betul, State Madhyapradesh (India) in 1990. He received the Bachelor of Engineering (B.E) in Electronics and Communication from Sagar Institute of Research and Technology, Bhopal in 2011 and Master of Technology (M.Tech.) from Maulana Azad National Institute of Technology, Bhopal in 2014. He got GATE scholarship given by Ministry of Human Resource and Development (MHRD), India for year July 2012 to June 2014. His research interest includes Design for manufacturability and reliability in deep submicron technology nodes, Physical design issues for CMOS Standard cell, High Speed & Low Power mixed signal design.